[existing on said wiring, and after extracting circuit information of said driver corresponding to one of said pair];

[extracting] identifying a segment that includes said high speed signal wiring and is nearest to said board edge from a group of segments [each defining a set of a minimum unit of a wiring configuration for said wiring];

[specifying] identifying a plane layer edge that is nearest, in a perpendicular direction, to a wiring between [a] the driver and [a] receiver [in said segment extracted];

determining a perpendicular distance between the wiring [extending from the driver to the receiver of said segment] and said plane layer edge;

computing a minimum interlayer distance required between a wiring layer of said segment [extracted] and said plane layer;

comparing said perpendicular distance [determined] and said interlayer distance computed; and

[displaying a message that contains a predetermined instruction corresponding to said wiring in accordance with a result of said comparison] identifying any undesirable aspects of said wiring.

REMARKS

Applicants thank the Examiner for the indication of acceptance of the drawings. Additionally, Applicants thank the Examiner for acknowledging Applicants' claim for foreign priority under 35 U.S.C. §119.

Applicants respectfully request reconsideration of the prior art rejections set forth by the Examiner under 35 U.S.C. §§102 and 103. Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicants' presently claimed invention. More specifically, Applicants' claimed

invention is directed to new and improved systems and methods for improving circuit layout design by identifying potential problems with a proposed layout or design based on the identification of potential problems arising from certain design characteristics that will likely lead to unacceptable electromagnetic interference problems or crosstalk based on the proposed circuit design.

Applicants note that the claimed technology is substantially different from that which is disclosed and described in the primary prior art reference upon which the Examiner relies in rejecting the claims. More specifically, the *Sasaki* reference, United States Publication No. US2001/0018761 is merely directed to a design assisting system. In this prior art system, the system initially determines the layout of parts information on the overall circuit board. This information is converted into a model for analyzing electromagnetic fields associated with the layout. See specifically, page 2 in paragraph 0021. At this point in the specification, the prior art reference states that this means for converting includes a means for specifying a frequency in calculating magnetic field intensity distribution near the ground plane using this model.

As understood by Applicants, all of the embodiments of this prior art reference utilize this technique which is different than that which is disclosed and claimed by Applicants in the present application. More specifically, Applicants approach is much different and uses the identification of wiring segments and specific layout parameters such as a distance from a nearest edge and so on. See specifically, Applicants claim 1, for example.

Applicants approach does not rely upon complex modeling algorithms for providing approximations or calculations as to EMI. Rather, Applicants have disclosed a far simpler approach to determining the appropriateness of a design.

The Examiner has asserted that the so called segment extraction unit for identifying a segment that is nearest to the board edge from a group of segments is described in paragraphs

75 and 80. Significantly, however, Applicants submit there is no teaching or suggestion whatsoever regarding the use of specific design parameters such as high speed wiring distances from the layout edges and so on, as set forth in Applicants present claims. More specifically, paragraph 75 merely states that for the purpose of analyzing an electromagnetic field, a specific analysis technique is utilized which defines the analytic space and divides the analytic space into small individual cells. The technique is used to sequentially calculate a time dependent change in the electromagnetic field in each of the cells. This obviously would take much more time than simply identifying a particular wiring element that is closest to an edge and then thereafter determining whether this will present a problem with high speed signal transmission. It would appear that far fewer calculations would be required. This is in contrast with the required calculation for a significant number of small individual cells as taught by the prior art.

Furthermore, paragraph 80 merely describes whether a given connection is capable of easily passing a common mode current through the ground plane or not and whether a particular interconnection is likely to become an unwanted radiation source or not. Neither of these paragraphs nor any other portions of the specification of the cited publication provide the required teaching or suggestion which would render applicants presently claimed invention obvious or anticipated.

In summary, Applicants have disclosed a novel approach to assist in determining whether a proposed design is desirable in light of electromagnetic interference concerns. Applicants technique does not rely upon modeling as in the prior art. Applicants claimed invention utilizes actual design parameters for rapidly determining whether a particular design is susceptible to EMI problems.

In light of the foregoing, Applicants respectfully request the Examiner now withdraw these rejections and allow all claims in the application.

Respectfully submitted,

Date: April 18, 2003

(Reg. #37,607)

Robert J. Depke
HOLLAND & KNIGHT LLC
131 South Dearborn Street, 30th Floor
Chicago, Illinois 60603
Tel: (312) 422-9050
Attorney for Applicants